Investigation of the Radio Frequency Characteristics of CMOS Electrostatic Discharge Protection Devices

T. M. Firestone, J. Rodgers, and V. L. Granatstein
Institute for Research in Electronics and Applied Physics (IREAP)
University of Maryland, College Park, MD 20742

Abstract

The input conductance of CMOS and many other integrated circuit technologies is determined mainly by the electrical properties of on-chip electrostatic discharge protection devices. Generally, they are designed to have diode-like characteristics to shunt potentially harmful static charge away from thin gate-oxide insulators. These nonlinear junctions may also rectify radio-frequency signals coupled onto CMOS data lines from incidental or malicious sources of interference. The rectification process generates down-converted voltages that may cause spurious response in the CMOS such as logic errors, persistent latching (upset), or undesirable shifts in logic levels. This paper presents a theoretical, numerical and experimental investigation of the radio-frequency characteristics of CMOS electrostatic protection. The inputs of commercial devices were excited by microwave pulses with the carrier frequency tuned near the parasitic resonance. The results show the regimes where microwave pulses cause state errors and unstable operating conditions in the circuit. In some devices, quality factors as high as four were measured, and upset occurred with carrier amplitudes as low as 350 mV. Good agreement between theoretical, numerical and experimental results is demonstrated, and a generalized approach to predicting radio-frequency effects in CMOS with electrostatic protection is introduced.

I. Introduction

Concern about compromised data and operational reliability in critical information systems due to radio-frequency (RF) effects has motivated studies of electromagnetic interference (EMI) and upset in electronic circuits. The EMI susceptibility of basic devices has been investigated for cases where the RF frequency was low enough to directly stimulate spurious circuit responses [1-4]. Various effects such as state errors and bias shift were studied for EMI frequencies in the range 1-300 MHz. The choice of this band was based on the assumption that devices are more sensitive to EMI that mimics valid logic waveforms. It has been widely reported that parasitic (shunt) capacitance in IC's decreases EMI effects for frequencies above 200 MHz. In [4], stray inductance was assumed to be negligible below about 3 GHz depending on the specific IC and package wiring. It was reported in [5] that the EMI susceptibility of CD4000 CMOS decreases with a nearly constant rolloff of 18 dB/ decade from 1-100 MHz. More recent test result (see Fig. 1) has shown that advanced high-speed CMOS is susceptible to EMI at microwave frequencies due to internal parasitic resonances.

Another effect that has been reported is simple rectification of EMI by semiconductor p-n junctions [5-9]. In such cases, voltages corresponding to the envelope of the RF carrier may be erroneously interpreted by logic gates as valid data. Tests on simple CMOS with on-chip electrostatic discharge (ESD) protection showed that pulse-modulated EMI affected susceptibility levels to an unspecified extent [4]. No causal mechanism was identified and the high-frequency characteristics of the circuits were not investigated in detail. Generally speaking, most of the published work reflects a phenomenological approach to the problem. Collections of test results for selected logic families (most nearing obsolescence) can be found in the literature [10]. In view of how rapidly semiconductor technology advances, the preferable approach would be to analyze the fundamental electronic mechanisms responsible for RF susceptibility in circuits and construct predictive models based on that understanding. If the problem can be defined in terms of basic, scalable circuit parameters, then electromagnetic compatibility can be considered in the design stage as new circuits are developed.

In this paper we present results from analysis, experiments and SPICE simulations from studies on the high-frequency characteristics of CMOS integrated circuits. It was

assumed that the input ESD protection circuits which consist of p-n junctions and other nonlinear devices have some capacity to rectify or otherwise respond to RF stimulus. High-frequency measurement techniques and analysis have been employed to study the response of advanced logic circuits to pulsed RF excitation. SPICE simulations were performed using models that include packaging, bond wire and bypass capacitor parasitics; and nonlinear device parameters obtained from both small and large-signal RF measurements. This paper is organized as follows. In Section II, a small signal analysis of RF detection by an ideal diode is presented. Some relevant high-frequency parameters are discussed, and the expected rectification voltages are calculated. The high-frequency characterization of the ESD protection devices are presented in Section III along with the measured transfer characteristics of a representative sample of advanced CMOS families. Section IV includes a discussion of the results and conclusions.

II. RF Characteristics of CMOS Inputs with ESD Diodes

In this chapter, a study of the high-frequency characteristics of ESD diodes using the conventions and techniques of microwave detector analysis will be presented. It will be demonstrated that ESD devices have significant sensitivity to RF excitation even though they are not designed for this purpose. Using the high-frequency characteristics of the diodes in SPICE models, it will be shown that good agreement between experimental and numerical results is achieved and that RF effects in circuits can be predicted with reasonable accuracy.

Figure 2(a) shows a schematic of typical CMOS input circuitry which consists of the parasitic lead and bonding wire inductance lumped into the parameter L_p, the ESD diodes connected to both the ground and V_{dd} power lines, and the first stage of complementary transistors. When the input is in the logic low state, the ground-clamp diode is biased closer to conduction than the power-clamp diode. As such we may simplify the analysis for now by considering the high-frequency behavior of the lower diode since it will conduct current at RF amplitudes which exceed the knee voltage, whereas conduction in the upper diode requires much higher RF amplitudes (at approximately the supply voltage, V_{dd}). A simplified circuit model is shown in Fig. 2(b)

where the ground-clamp diode has been replaced by an equivalent network including the current-spreading resistance R_s and a junction capacitance C_j shunted by a resistance $R_V = 1/G_d$, where G_d is the dynamic conductance of the diode. When the bias voltage is zero, $R_V = V_T / I_S$, where $V_T = kT/q$ is the thermal voltage, I_S is the diode saturation current, k is Boltzmann's constant, T is Kelvin temperature and q is the elemental electron charge. In the figure, C_j and R_V are shown as variable elements because they both depend on the diode voltage V_d and are therefore dynamic quantities. It can be immediately seen that the network has a second-order transfer characteristic which is given in Laplace notation (stimuli with time dependence e^{-st} and complex frequency $s = \alpha + j\omega$) by

$$\frac{V_d}{V_{in}} = \frac{1 + sC_jR_S}{1 + s^2L_PC_j + sC_jR_S}. \tag{1}$$

When the circuit is driven at the resonant frequency $f_R = 1/2\pi\sqrt{L_pC_j}$, the transfer function reduces to

$$V_d / V_{in} = 1 - j\sqrt{L_P / C_j} / R_S. \tag{2}$$

Typical values for R_s, C_j and L_p in advanced CMOS are roughly in the ranges 3-20 Ω, 2-5 pF and 4-10 nH, respectively. Thus, CMOS commonly exhibit resonances somewhere between 500 MHz and 1.8 GHz, and V_d / V_{in} may be as high as a factor of six depending on the value of R_s. In some IC packages, the inductance of the ground and power supply leads is significant as well. In these cases, the transfer function would contain higher order poles and zeros since the return path for RF current may flow in either or both of these circuit nodes. For now, we will assume that the ground return is ideal and compare results from measurements and the simplified model. Passive voltage gain and increased RF susceptibility due to parasitic oscillation in IC's has not been previously reported. We note that the above values account only for internal parasitic reactance, not loading due to printed traces and the surrounding circuitry.

Commercial HCT (14-pin DIP) hex CMOS inverters were chosen for testing purposes because they are widely used in digital systems to convert TTL into CMOS-

compatible levels. The on-chip ESD device between the input and ground line in the HCT consists of a comparatively large (~2 micron) NMOS transistor with its gate tied to ground. In Fig. 1(a), the diodes connected from the input to either or both the ground and supply lines establish two basic pathways for RF current, each with a voltage-dependent dynamic impedance. During normal operation, the junction biases would change constantly as valid logic waveforms arrive at the inputs. Depending on the coincidence of an RF pulse with respect to the logic voltage, the diodes would be driven at varying operating points along their respective current-voltage (I-V) curves. In the present work, we did not consider time-varying bias; instead, the input was assumed to be a constant DC voltage which is consistent with the manufacturer specified input logic low (V_{il}) and high (V_{ih}) voltage levels.

Once the high-frequency parametric curves $C_j(V_d)$ and $R_V(V_d)$, and the constant terms R_s and L_p are known for a given diode network, its sensitivity to RF excitation should be predicted by lumped element models. This hypothesis was tested by measuring the DC and high-frequency characteristics of the HCT input diodes, constructing PSPICE models using circuit parameters extracted from the small-signal test data and by comparing the results of the simulations with large-signal experiments.

A. DC and High-Frequency Characteristics of ESD Diodes

In the following, the experimental measurement of the diodes and determination of the high-frequency circuit parameters are discussed. The IC packages were mounted on printed circuit boards with their inputs fed by SMA-type RF connectors soldered approximately 5 mm from the input pin. The DC I-V characteristics of the input diodes were measured using a semiconductor curve tracer. Shown in Fig. 2 is a plot of the experimental data compared to the expression for the current-voltage relationship in an ideal diode given by $I_D = I_S[\exp(-V_d / nV_t) - 1]$. Here, I_S is the forward saturation current, V_d is the applied voltage, *n* is an ideality factor related to the type and concentration of doping in the junction and the other terms are defined above.

The high-frequency impedance of the HCT input was measured using an HP8722D vector network analyzer (VNA) equipped with an internal bias circuit.

Measurement data were digitally recorded for frequency sweeps between 50 MHz to 6 GHz and for bias voltages between 0-3 V (the specified range of input logic voltages). The VNA averaging function was enabled in order to eliminate noise in the measurements. At test frequencies below about 100 MHz, the phase of input impedance was purely capacitive as evidenced by , and the data was fitted to the equation $C_{in} = C_S + C_{j0}(1+V_d / V_j)^{-m}$, which describes the capacitance-voltage relationship of an input consisting of an ideal junction in parallel with stray capacitance C_S. using a numerical least-squares regression to obtain the parameters C_{j0}, V_j and *m* which are the zero-bias junction capacitance, the junction potential, and the emission coefficient, respectively. The parasitic inductance was calculated from the measured angular resonant frequency ω_R and junction capacitance using $L_p = 1/\omega_R^2 C_j$. The imaginary part of the impedance (reactance) vanishes at ω_R, and the remaining real impedance is R_s, gives the current-spreading resistance in series with the high-frequency skin resistance of the IC leads. Figure 4 shows the magnitude of the impedance versus frequency with the input biased to V_{il} and V_{ih}. A summary of the diode parameters is given in Table I.

B. Measured and Simulated Large-Signal RF Response of ESD Diodes

The large-signal response of the HCT was measured as follows. Figure 5 shows a schematic of the test system including the instrumentation, RF path and circuit nodes at which voltage measurements were taken. A Stanford Research Systems DG535 pulse generator supplied pulses to synchronize a digital oscilloscope and serve as the modulation input to the Agilent E4438C RF signal generator. The pulse width and repetition frequency were 10 μsec and 100 Hz, respectively. The carrier frequency of the signal generator was tuned in each case to the parasitic resonant frequency as discussed above. A bias Tee, rendered in the figure as a coupling capacitor on the RF port and a low-pass filter (LPF) on the bias port, was inserted into the RF path between the generator and the device under test (DUT). The bias port served as a low-pass node for applying DC voltages and making measurements of the voltage response of the diodes to

pulsed RF. The LPF cutoff frequency of 100 MHz determined the maximum measurement bandwidth of voltage waveforms which were down-converted off the carrier by diode rectification. This voltage was measured across a 10-kΩ resistor, which also served to bias the DUT to defined logic states. Figure 6 shows a typical input response waveform when an RF pulse was applied to the HCT. It can be seen that the ESD diodes produce a fairly good representation of the RF envelope. The voltage measurements were averaged over the flat (top) portion of the pulse and digitally recorded for each step in carrier amplitude between 20 mV and 1.0 V in 20-mV increments and carrier frequency between 200 and 1500 MHz in 2-MHz increments. The devices were powered using a regulated 3.3 VDC supply, and 0.2 μF ceramic bypass capacitors were soldered as close as possible between the supply and ground terminals. Device response was measured with the 10-kΩ input resistor grounded and also fed from a regulated 3.0-VDC voltage source to simulate device operation in both the low and high logic states, respectively. We note that for RF amplitudes below approximately 200 mV no response was observed. This is a reasonable result since the RF voltage must exceed V_j over some portion of its cycle in order for the diode to conduct and rectify. The onset of rectification at 200 mV was evidence that the oscillating voltage across the diode was higher due to the quality factor in the circuit. In the HCT, V_j = 0.65 V which means that the voltage gain as defined in (2) is $V_d / V_{in} \sim 0.65 / 0.200 = 3.25$ about 3.25. Substituting the HCT diode parameters R_s =15 Ω, C_{j0} = 5.8 pF and L_p = 16 nH from Table I into (2) yields a theoretical gain of 3.64, which is in good agreement with the above estimate. Shifts in the resonant frequency and the quality factor of the circuit, which appeared implicitly in (2) as $V_d / V_{in} = 1 - jQ$ where $Q = \sqrt{L_p / C_j} / R_s$, were observed as the RF drive parameters were varied. This observation provided evidence that voltage gain and rectification response of the circuit is both dynamic and affected by the rectification voltage.

The circuits were simulated using PSPICE with the high-frequency parameters given in Table I applied to the diode models and the parasitic elements. Figure 7 shows the circuit model which includes the parasitic inductance, input diffusion resistance, CMOS transistors arranged in triple-buffered configuration, the bias circuit and the

equivalent series resistance of the bypass capacitor. Transient analysis was performed for the same range of RF amplitudes as in the experiments and with the inputs biased to both V_{il} and V_{ih}. The time necessary for the input response voltage to reach steady state in the simulation was about 500 nsec, and the computation time on dual-processor workstation was approximately two minutes. Figure 8 shows a comparison of the input response voltage versus RF amplitude from the measurements and simulations when the frequency was tuned to the zero-bias resonance of the HCT. We note that the CMOS transistors used in the simulations were unmodified library models. In the future, a study of the high-frequency characteristics of CMOS will be conducted so that improved transistor models may be included in the simulations. Nevertheless, the models give fairly good agreement for the case studied here.

C. Dependence of RF Sensitivity on the Video and External Load Resistance

Recall that in the numerical and experimental circuits a value of 10 kΩ was chosen for the input bias resistor purely based on bias and logic considerations. Essentially, the above results give the RF transfer characteristics for a single, static load condition. In reality, the inputs to CMOS devices are loaded by the preceding circuitry, which itself changes states (output impedance) as the desired logic waveforms are generated. Also, recall that the model of an RF detector diode (see Fig. 1(b)) includes $R_V(V)$ the dynamic video resistance which is essentially the inverse RF conductance of the junction. This parameter depends on the I-V characteristics of the device which, in turn, determines its sensitivity to the RF voltage v_{rf}. In the small-signal limit where $V_0 >> v_{rf}$, the rectified voltage V_d can be expressed by the Taylor series

$$V_d = Z_L I_d(V) = V_0 + Z_L \sum_{n=0}^{\infty} \frac{v_{rf}^{n+1}}{(n+1)!} \frac{d^n G_d}{dV^n}. \qquad (3)$$

In the above expansion, V_0 is the DC bias point, which in our case is the logic voltage applied to the input, Z_L is the impedance the diode current sees, and G_d is diode conductance. We have expressed the load as an impedance to account for the general case where it may be complex. In the following, we will assume that the load is purely resistive and solve (3) using a small-signal approximation, namely, that the second

derivative of the conductance curve is reasonably constant over voltage excursions with amplitude v_{rf}. The detected voltage for the case where $V_0 = 0$ following the analysis in [13] is

$$V_{\mathrm{d}} = Z_L I_d = Z_L \frac{{v_{rf}}^2 I_s}{4V_t^2}. \tag{4}$$

The v_{det} measurable voltage at the terminals, is the drop across the external load resistor R_L where $Z_L = R_L \,||\, R_V$ and is given by

$$v_{det} = \frac{{v_{rf}}^2 I_s}{4V_t^2} \frac{R_L R_V}{R_L + R_V}. \tag{5}$$

From (4) and (5) it can be seen why RF diodes are commonly called "square-law" detectors since $v_{\mathrm{det}} \propto v_{rf}^2$.

To test the validity of the analysis, the bias resistor in the experiments and simulations was varied by decades from 100 Ω to 1MΩ and from 100 Ω to 1MΩ in 500 points, respectively. Figure 9 shows a plot of v_{det} from theory (with the diode parameters substituted into the relevant variables), simulations and the experiments versus load conductance $G_L = 1/R_L$.

III. Transfer Characteristics of CMOS Driven by Pulsed RF

In the previous chapter, the behavior of ESD diodes was considered apart from the operation of the circuit as a whole. In this chapter we extend the analysis is applicable to a wide variety of devices and forms the basis for predicting RF effects in IC's in general. In this chapter, a study of the effects RF pulses have on the operation of CMOS devices is presented. Before proceeding, it will be instructive to briefly consider the special case when amplitude-modulated (AM) RF carriers are rectified (detected) by diodes.

When junctions are excited by an AM carrier, rectification produces a voltage which contains harmonics of the carrier frequency plus a reconstructed version of the low-frequency AM signal. For the special case of steady-state sinusoidal modulation the detected voltage after low-pass filtering is written

$$v_{det}(t) = i_D(t)Z_L = \frac{Z_L v_{RF}^2}{4} G'(1 + \frac{m^2}{2} + 2m\cos\omega_m t + \frac{m^2}{2}\cos 2\omega_m t), \quad (6)$$

where ω_m and *m* are the AM frequency and modulation index when the constraints $\omega_m << \omega_{RF}$ and 0<m<1, respectively, hold true. When the RF is carrier pulsed, its spectrum contains modulation sidebands with Fourier amplitudes that follow an envelope function given by $A(\omega) \propto \sin\omega_m / \omega_m$. Equation (6) still applies as long as the Fourier coefficients of all sideband frequencies are computed. Since rectification is a nonlinear process, the diodes generate harmonic products of the pulse and carrier frequencies, all of which appear at the CMOS gates. The condition $\omega_m << \omega_{RF}$ implies that the gate stimulus will occupy two distinct frequency bands 1) the modulation frequencies, which we will assume are within the normal gain-bandwidth of the CMOS transistors and 2) the RF frequencies, which may be amplified or attenuated by the CMOS depending on the high-frequency characteristics of the transistors. Here, we will consider the demodulated waveform as the principal cause of effects in the CMOS. As such, the response voltages were measured over a bandwidth that encompasses the AM spectrum only. Note that sometimes a remnant of the RF waveform with significant amplitude was visible at the output of the device when time-averaging was removed and the measurement bandwidth was increased.

The measurements of the HCT response were conducted as described before using the test system shown in Fig. 5 with the carrier tuned to the parasitic resonant frequency of the DUT. Since the internal circuit, the rectified voltage can be higher than predicted by (6). As the RF amplitude was increased in 20 mV increments, the output voltage and supply current was measured with the input biased to the low and high states. The input and output voltages and the supply current waveforms were recorded by a digital oscilloscope using a Tektronix P6243A probe across the 10-kΩ input bias resistor and a Tektronix P6139A probe across a 1.0-MΩ resistor at the output terminal. The RF pulse width was 10 μsec which gave adequate time for the response voltages to reach steady state before the pulse terminated. To reduce noise and fluctuation in the data, the digitized voltages and current were averaged over a time window of 5 μsec which was

centered on the flat portion of the pulse. The bandwidth of the voltage measurements was limited to 20 MHz by the frequency response of the oscilloscope.

PSPICE simulations were performed to verify that the circuit models of the ESD diodes and CMOS transistors predicted the measured response characteristics with reasonable accuracy. Transient analysis was performed for a simulation time of 6 μsec using a step ceiling of 50 psec. The simulated RF-pulse width was narrower than in the measurements to save simulation time. A comparison of the input and output response voltages versus time from measurements and simulations of the HCT circuit in both bias states is shown in Figs. 11. Waveforms were recorded for RF amplitudes of 0.4 and 1.0 volts to demonstrate the cases where the input response voltage is above and below the CMOS threshold voltage where the logic state changes. The complete data sets for the HCT and LVX devices are shown in Figs. 13 and 14 represented as voltage and current transfer curves versus RF amplitude.

In Fig. 13(a), the data for HCT response with its input biased low indicates that RF amplitudes above 0.38 V cause the output to latch low. The abrupt spike in supply current is consistent with normal operation in CMOS since both the NMOS and PMOS transistors conduct when the input voltage is near the switching threshold. Evidently, the envelope voltage from the rectified RF pulse has mimicked a valid logic waveform and induced a state error in the device. A more subtle effect is the elevated leakage current of about 1 mA for RF amplitudes higher than about 0.4 volts. This result indicates that not all the transistors are completely latched in their respective states. Rather, a high-frequency current continues to flow through the source-drain channel of the input buffer and possibly the second gain stage. In Fig. 13 (b), the data shows that biasing the HCT high produces a very different result. In this case, the bias condition forces the RF current to flow through the (upper) diode with its anode connected to the input through a diffusion resistance and the cathode to the power bus. The impedance of this network is higher and, as previously discussed, the dynamic capacitance is different which means that the resonant frequency and response characteristics have been altered by the bias. We note that the RF carrier in all the measurements was tuned to the zero-bias resonant frequency. Nevertheless, the RF still causes the output voltage to rise slightly meaning

that the output transistors are biased towards conduction. The current transfer characteristic is very nonlinear around RF amplitudes of about 0.65 volts.

The data in Figs. 14 (a) and (b) show that the LVX has a much smoother transfer curve and that state errors occur only with the input biased high and RF amplitudes above approximately 1.35 V. When the input is biased low, the RF causes the output transistors to partially conduct as evidenced by the minima in voltage and maxima in the current curves at around 1.2 V of RF drive. Figure 15 illustrates the mapping of measured input and output responses versus excitation amplitude and frequency. It can be observed that the voltage-dependence of the junction capacitances causes an upshift in the resonant response. Since the rectified voltage has a nonzero mean, it constitutes a new bias condition which decreases the junction capacitance. Thus, excitation at frequencies significantly above the zero-bias resonance still produces substantial gain and increases the likelihood of upset over a fairly wide bandwidth.

V. Discussion and Conclusions

Concerning the accuracy of the numerical models, a major drawback was not having the ability to measure the high-frequency characteristics of the MOS devices and implement those parameters in the model. In lieu of this information, the transistors were modeled using Level 4 SPICE models based on 1.2 um MOSIS MOSFETS with characteristics that accurately predict their behavior when the stimulus is a normal logic waveform. The models have not been tested when the input excitation consists of combinations of DC, AM, carrier harmonics and inter-modulation products. The data demonstrates that the transistor models do not predict some of the effects that have been observed in the experiments. In future work, high-frequency measurements will be performed on unpackaged CMOS transistors in order to evaluate which parameters are lacking or require modification in the circuit models.

The response of the HCT and LVX CMOS inverters to pulsed RF excitation has been studied where effects are caused by rectification of the RF by ESD protection diodes. The high-frequency characteristics of the diodes have been measured and successfully implemented in SPICE models, which have been shown to predict the RF

transfer curves of the diodes. The dynamic nature of the circuit parameters and their importance with respect to circuit response has been discussed, calculated and compared with experimental results with good agreement. Passive gain due to parasitic oscillations in the input networks has been shown to increase susceptibility when devices are excited near and above their zero-bias resonant frequency. In the HCT experiments, a passive gain of 3.25 was demonstrated which compared favorably to the theoretical value of 3.64. Finally, the output voltage and current transfer curves have been measured, and the conditions leading to logic-state errors, partial conduction and excess current draw have been studied and characterized.

Acknowledgements

The authors would like to thank Prof. Steve Anlage for many informative discussions and his encouragement in this work. Ron McLaren designed and constructed many of the test circuits and wrote code for the RF control and diagnostic system. This work is sponsored by the Air Force Office of Scientific Research (AFOSR) under the MURI contract F496 200 110 374.

References

1. (Todd's Conference paper)
2. M. L. Forcier and R. E. Richardson, Jr., "Microwave-rectification RFI response in field-effect transistors," *IEEE Trans. Electromag. Compat.*, vol. EMC-21, no. 4, Nov. 1979.

3. K. Gong, H. Feng, R. Zhan, and A. Z. H. Wang, "A Study of Parasitic Effects of ESD Protection on RF ICs," *IEEE Trans. Microwave Theory and Techniques*, Vol. 50, No.1, January 2002.

4. D. J. Kenneally, D. D. Wilson, and S. Epshtein, "RF upset susceptibilities of CMOS and low power Schottky 4-Bit magnitude comparators", *1990 IEEE Int. Symp. on Electromag. Compat.*, Wash. DC, 21-23 Aug. 1990, pp. 671-677.

5. D. J. Kenneally, D. S. Koellen, and S. Epshtein, “RF upset susceptibilities of CMOS and low power Schottky D-Type, Flip Flops,” *Rec. 1989 IEEE Nat. Symp. Electromag. Compat.*, Denver, CO, 23-25 May, 1989, pp. 190-195.

6. D. J. Kenneally, G. O. Head, and S. C. Anderson, “EMI noise susceptibility of ESD protect buffers in selected MOS devices,” *Procs. IEEE Int. Conf. on Electromag. Compat.*, Wakefield, MA, August 1985, pp. 251-261.

7. R. Richardson, “Microwave rectification of RFI in logic circuitry,” *NBS Conf. Microelectronics and Electromag. Susceptibility*, Gaithersburg, MD, 12-13 Mar., 1985.

8. R. E. Richardson, Jr., “Quiescent operating point shift in bipolar transistors with AC excitation,” *IEEE J. Solid-State Circuits*, vol. SC-14, no. 6, Dec. 1979.

9. S. D. Le Vine and R. E. Richardson, “Measurement techniques and instrumentation for determining sensitivity of digital IC’s to radio-frequency interference,” *Proc. ITMC/86, IEEE Instrum. Meas. Tech. Conf.*, Boulder CO., March 25-27, 1986.

10. J. N. Roach, “The susceptibility of a 1k NMOS memory to conducted electromagnetic interference,” *Rec. 1981 Nat. Symp. Electromag. Compat. Symp.*, Boulder, CO, Aug. 1981, pp. 85-90.

11. G. Sketoe, “Integrated Circuit Electromagnetic Immunity Handbook”, *Boeing Information, Space and Defense Systems*, Seattle, WA, August 2000.

12. Albert Z. H. Wang, *On-chip ESD Protection for Integrated Circuits*. Norwell, MA, Kluwer, 2002.

13. J. J. Whalen, J. G. Tront, C. E. Larson and J. M. Roe, “Computer aided analysis of RFI effects in digital integrated circuits,” *IEEE Trans. Electromag. Compat.*, vol. 21, pp. 291-297, Nov. 1979.

14. D. M. Pozar, *Microwave Engineering, 2nd ed.*, New York, NY: J. Wiley & Sons, 1998.

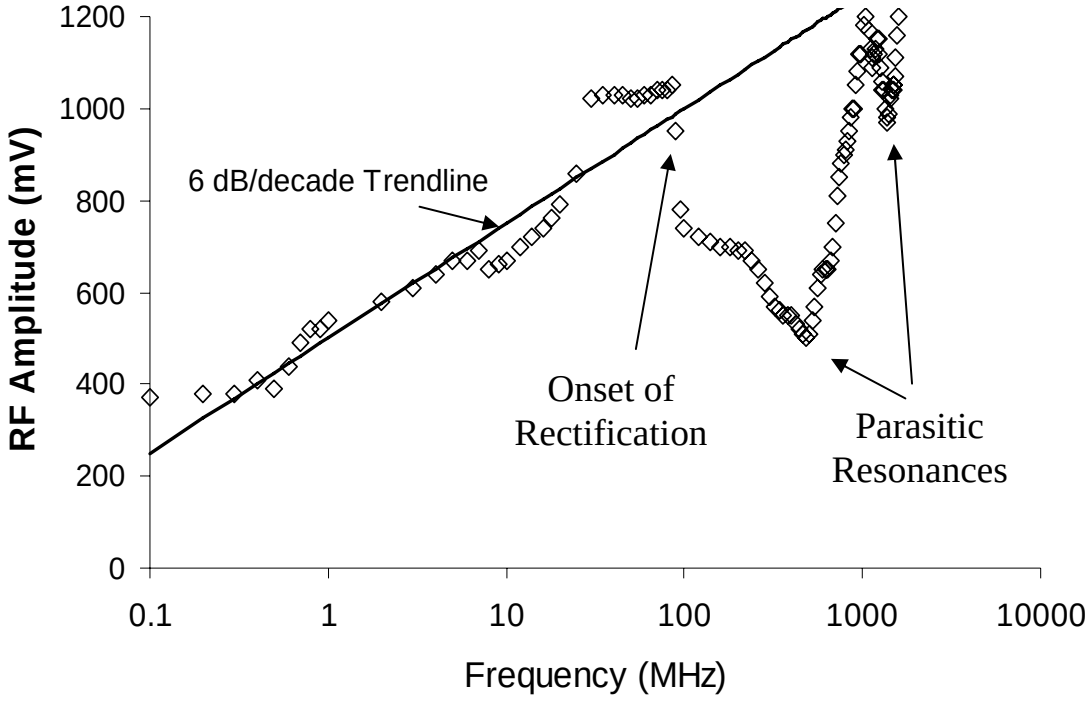
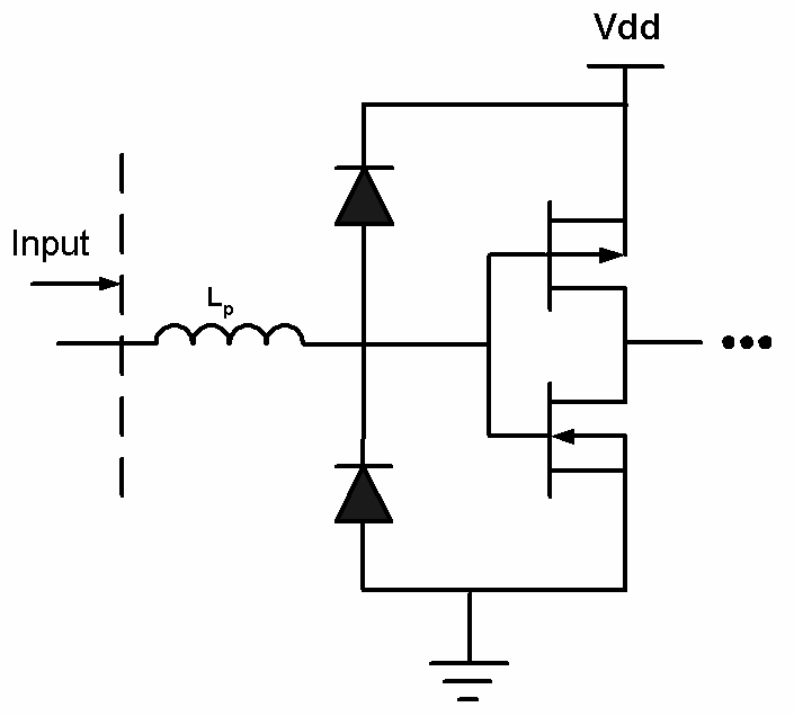
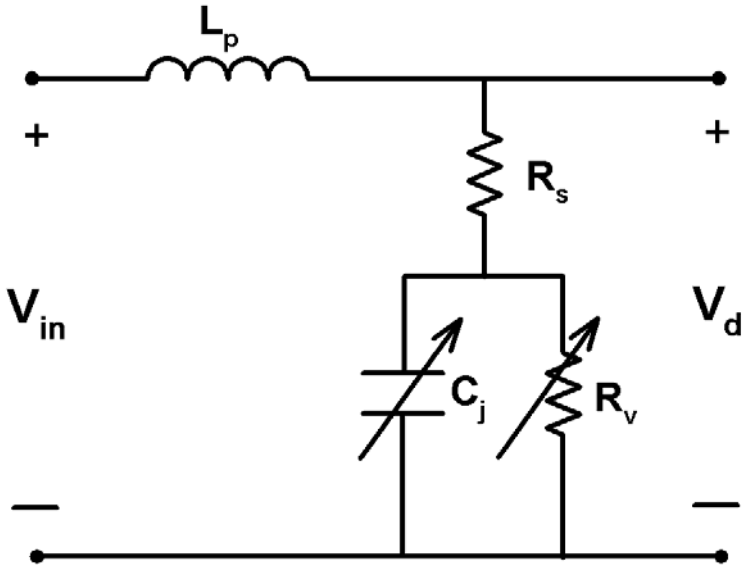

1200
1000
800
600
400
200
0
RF Amplitude (mV)
6 dB/decade Trendline
Onset of
Rectification
Parasitic
Resonances
0.1
1
10
100
1000
10000
Frequency (MHz)

Fig. 1



(a)



(b)

Fig. 1

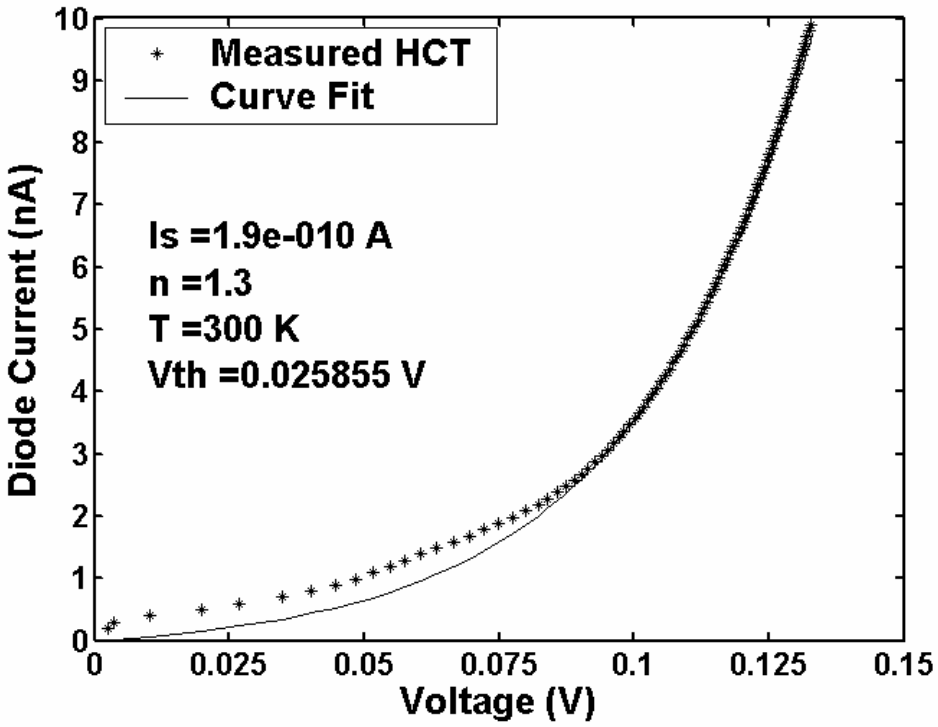

Measured HCT
Curve Fit
Is =1.9e-010 A
n =1.3
T =300 K
Vth =0.025855 V
Diode Current (nA)
Voltage (V)
0
1
2
3
4
5
6
7
8
9
10
0
0.025
0.05
0.075
0.1
0.125
0.15

Fig. 2

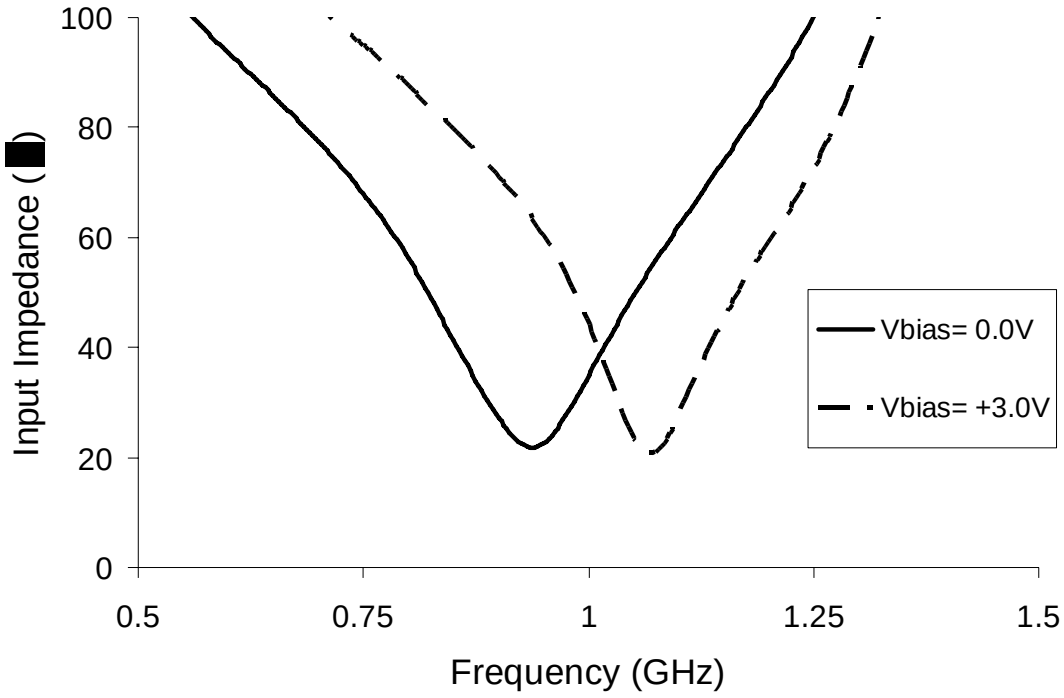

100
80
60
40
20
0
Input Impedance ( )
0.5
0.75
1
1.25
1.5
Frequency (GHz)
Vbias= 0.0V
Vbias= +3.0V

Fig. 3

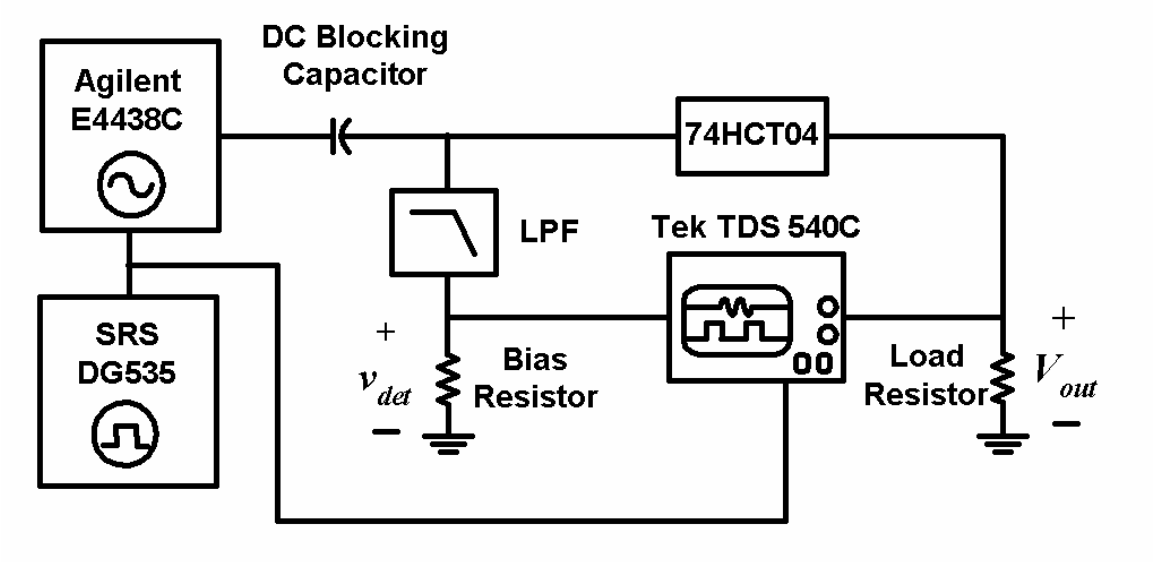

Agilent
E4438C
DC Blocking
Capacitor
74HCT04
LPF
Tek TDS 540C
SRS
DG535
+
v_{det}
−
Bias
Resistor
Load
Resistor
+
V_{out}
−

Fig. 4

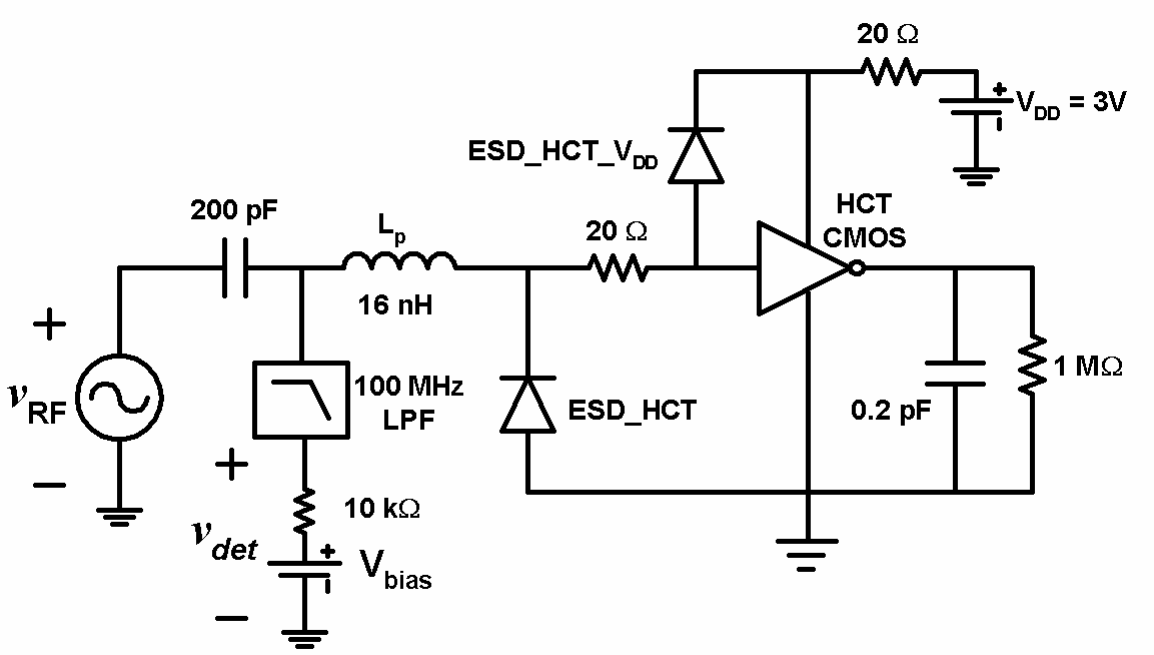

20 Ω
V_{DD} = 3V
ESD_HCT_V_{DD}
HCT
CMOS
200 pF
L_p
20 Ω
16 nH
v_{RF}
100 MHz
LPF
ESD_HCT
0.2 pF
1 MΩ
10 kΩ
v_{det}
V_{bias}

Fig. 6

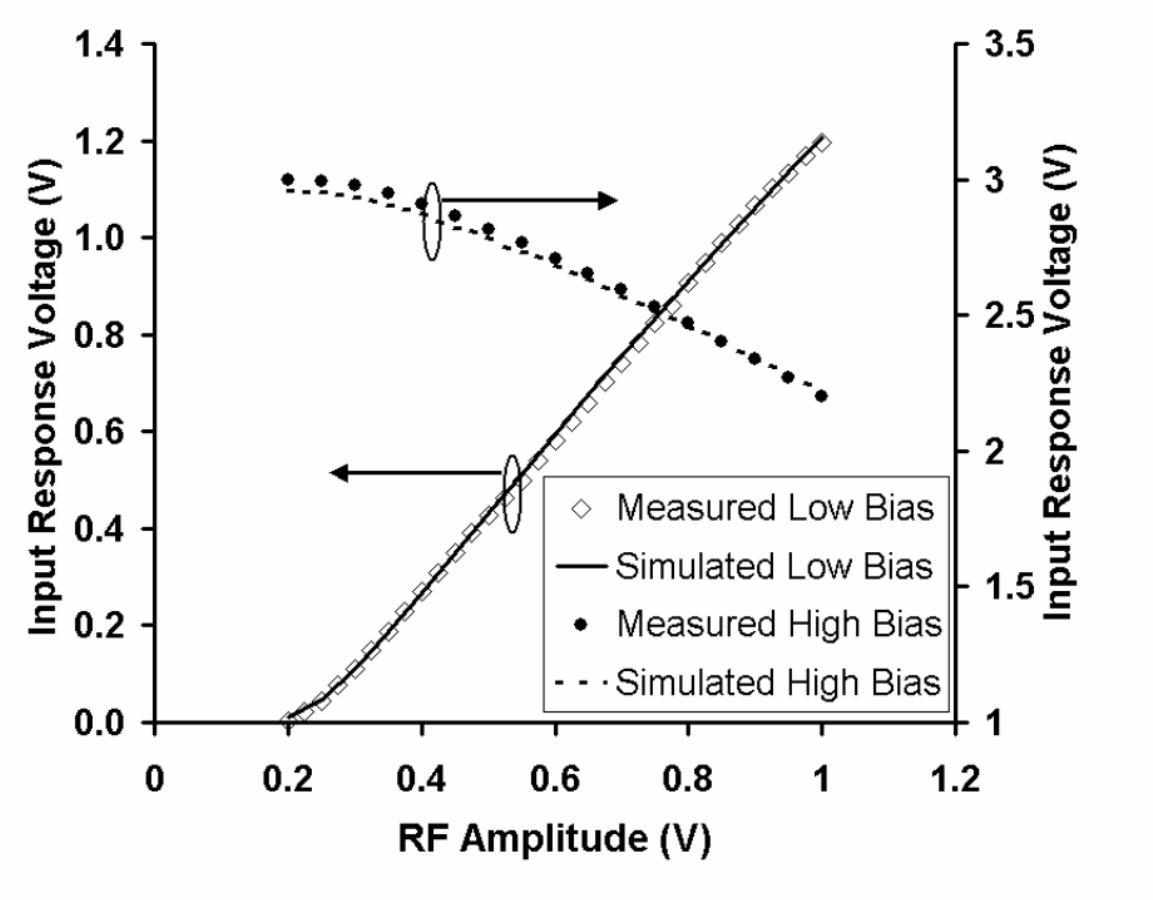

Input Response Voltage (V)
Input Response Voltage (V)
RF Amplitude (V)
Measured Low Bias
Simulated Low Bias
Measured High Bias
Simulated High Bias
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1
1.5
2
2.5
3
3.5
0
0.2
0.4
0.6
0.8
1
1.2

Fig. 7

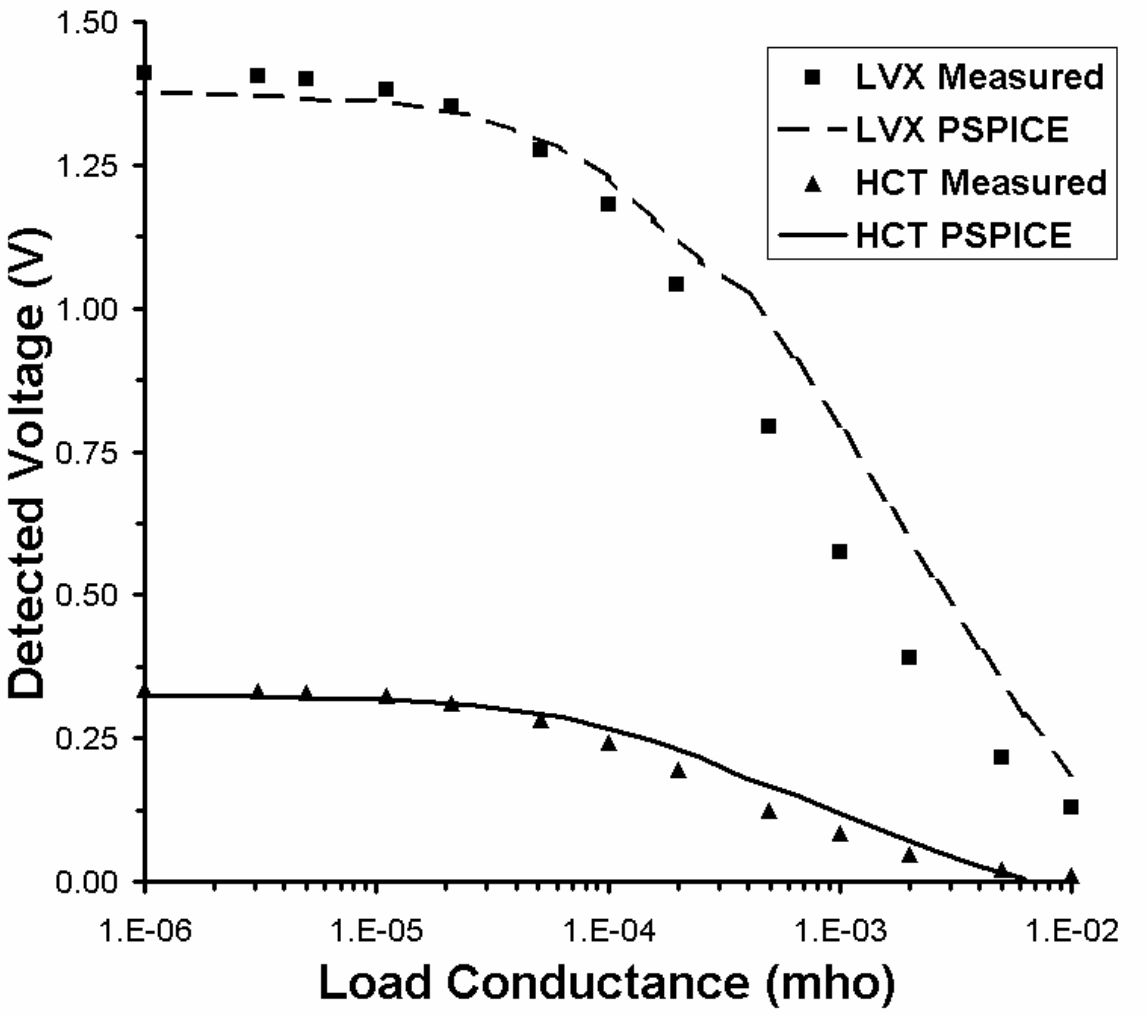
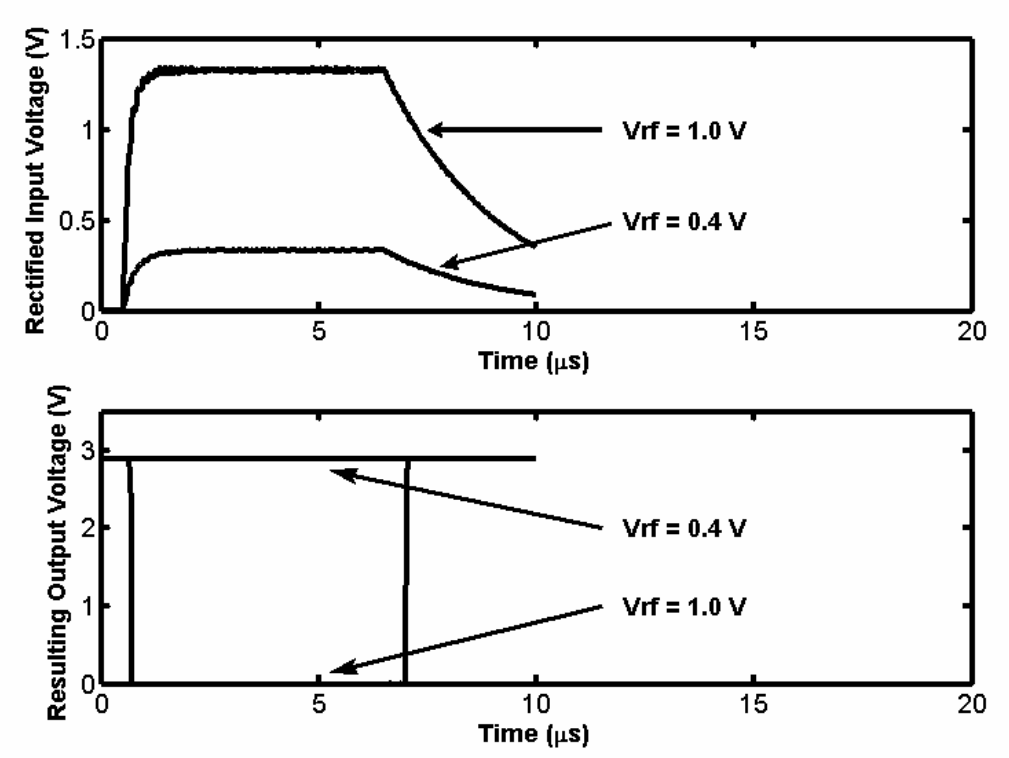
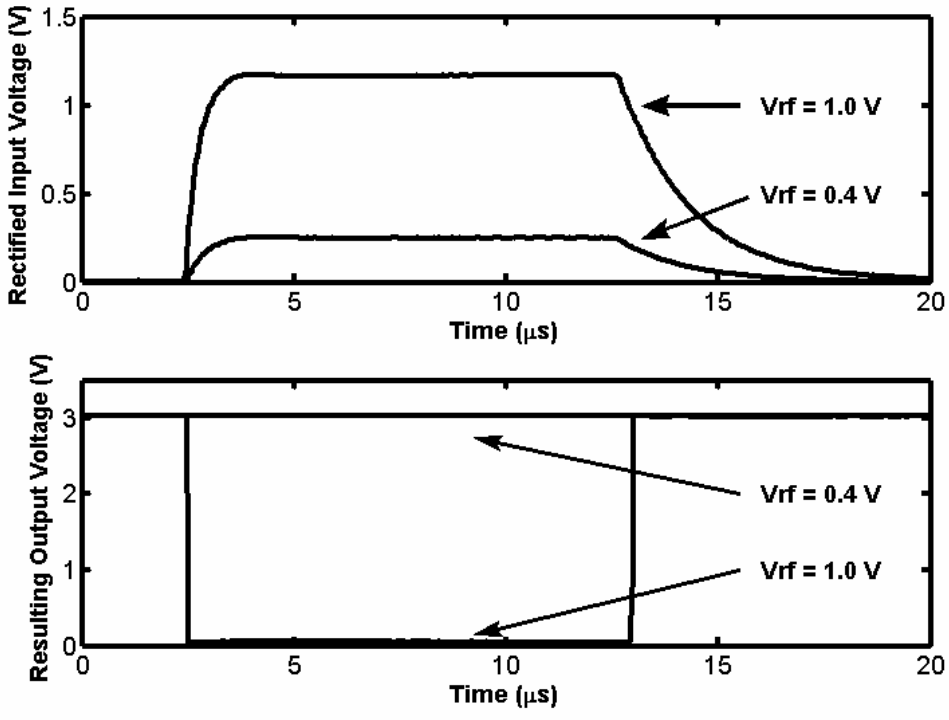

LVX Measured
LVX PSPICE
HCT Measured
HCT PSPICE
Detected Voltage (V)
1.50
1.25
1.00
0.75
0.50
0.25
0.00
1.E-06
1.E-05
1.E-04
1.E-03
1.E-02
Load Conductance (mho)

Fig. 10

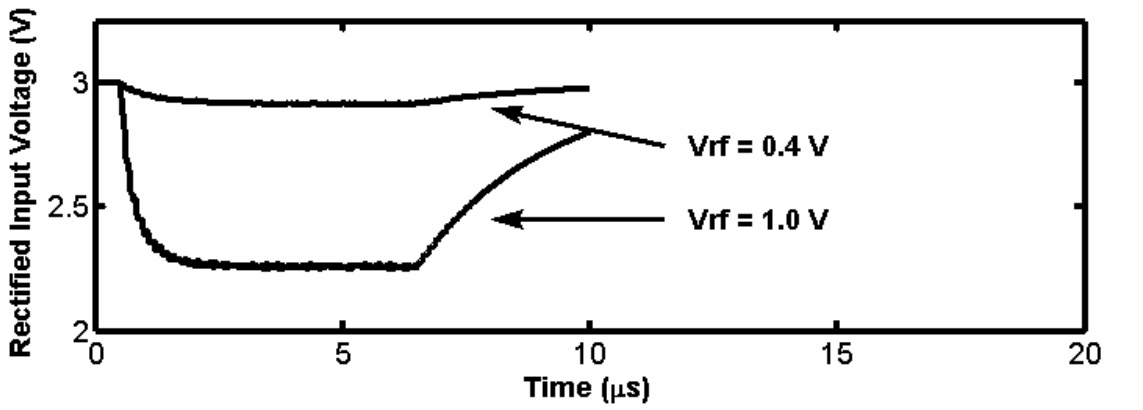

Rectified Input Voltage (V)
1.5
1
0.5
0
0
5
10
15
20
Time (μs)
Vrf = 1.0 V
Vrf = 0.4 V
Resulting Output Voltage (V)
3
2
1
0
0
5
10
15
20
Time (μs)
Vrf = 0.4 V
Vrf = 1.0 V

(a)

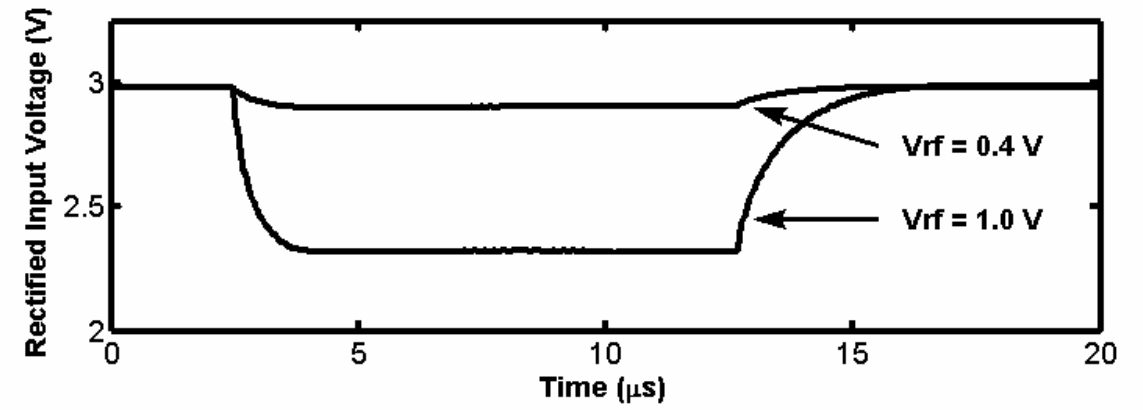

Rectified Input Voltage (V)
1.5
1
0.5
0
0
5
10
15
20
Time (μs)
Vrf = 1.0 V
Vrf = 0.4 V
Resulting Output Voltage (V)
3
2
1
0
0
5
10
15
20
Time (μs)
Vrf = 0.4 V
Vrf = 1.0 V

(b)

Fig. 11


Rectified Input Voltage (V)
3
2.5
2
0
5
10
15
20
Time (μs)
Vrf = 0.4 V
Vrf = 1.0 V

(a)


Rectified Input Voltage (V)
3
2.5
2
0
5
10
15
20
Time (μs)
Vrf = 0.4 V
Vrf = 1.0 V

(b)

Fig. 12

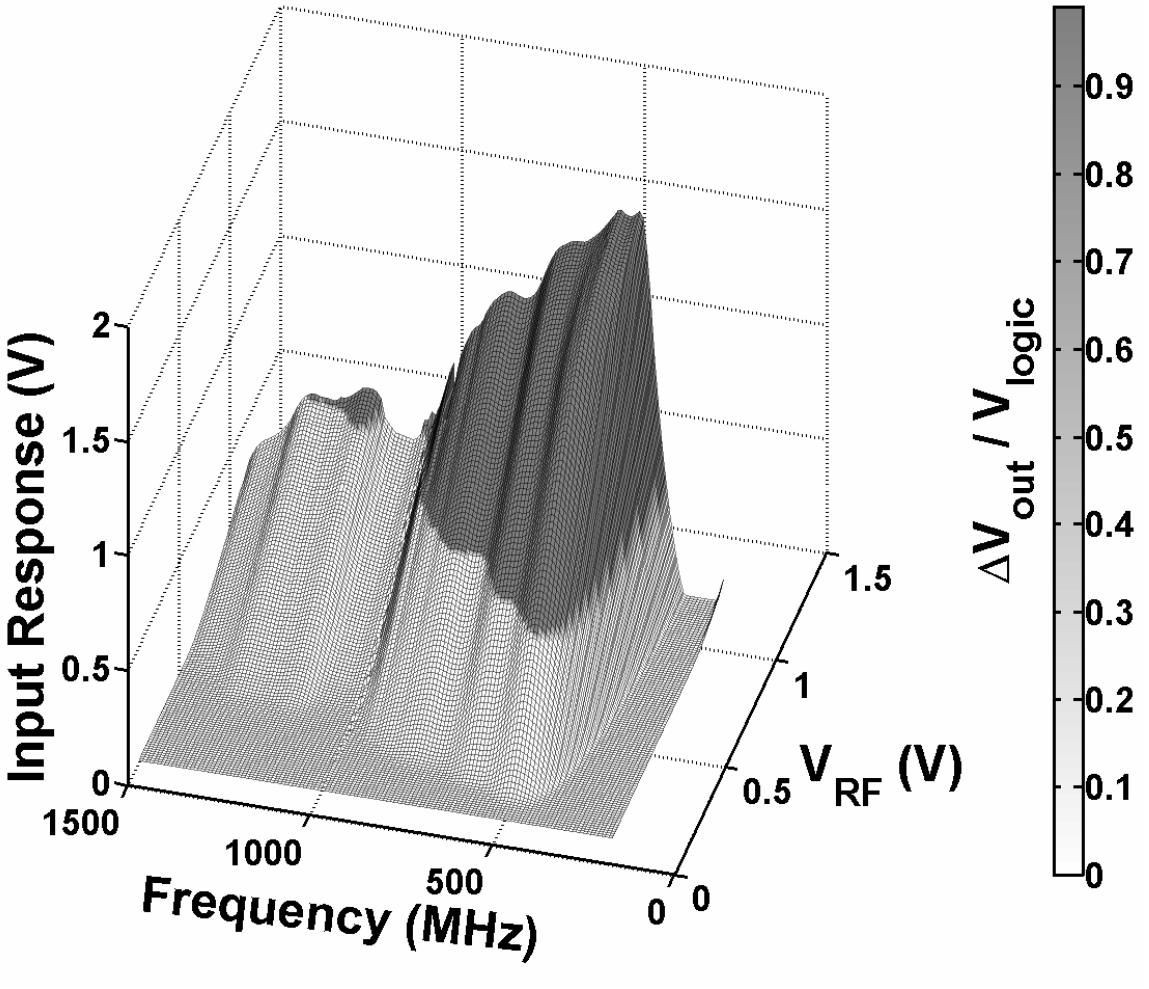

Input Response (V)
2
1.5
1
0.5
0
1500
1000
500
0
Frequency (MHz)
0
0.5
1
1.5
V_RF (V)
ΔV_out / V_logic
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

Fig. 13

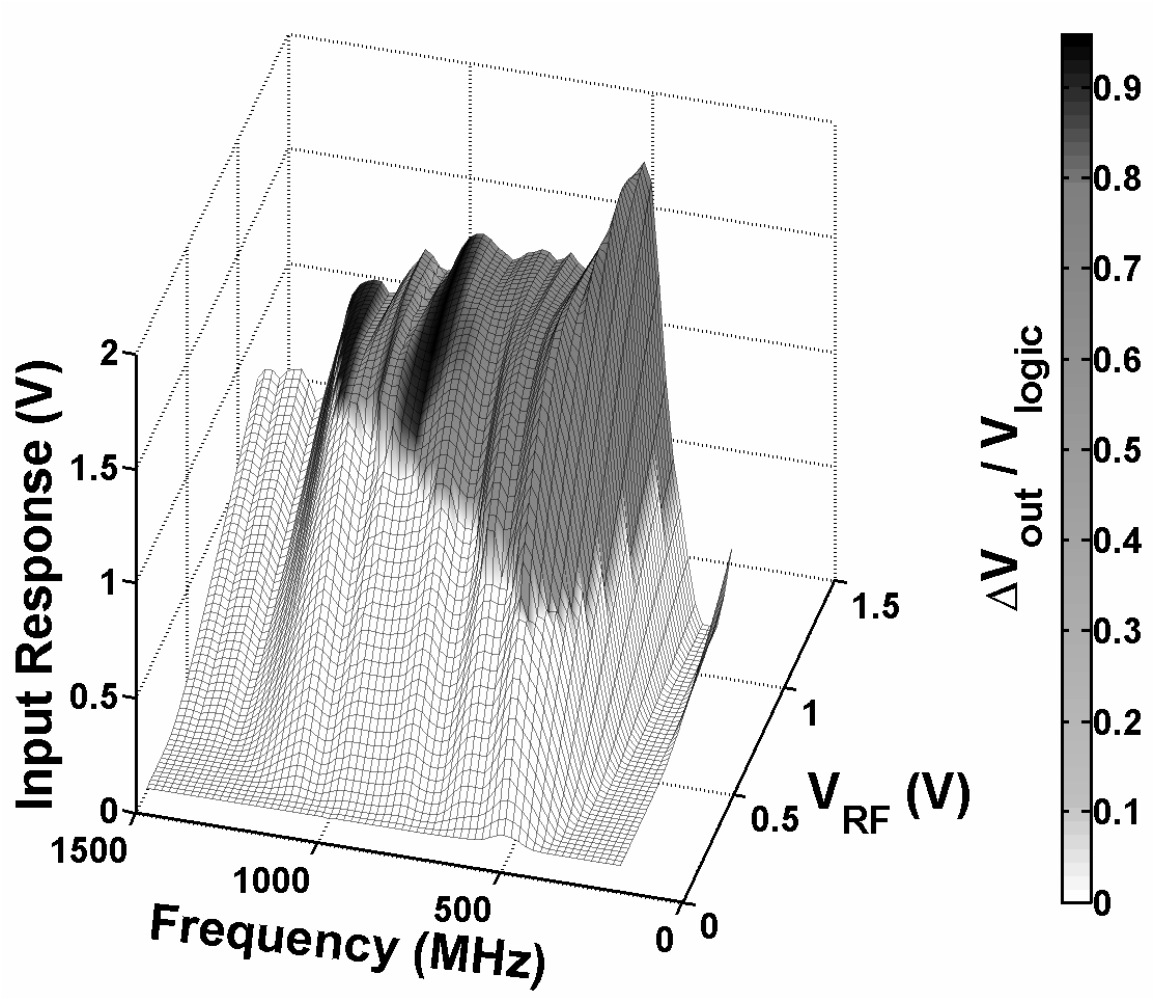

Input Response (V)
2
1.5
1
0.5
0
1500
1000
500
0
Frequency (MHz)
0
0.5
1
1.5
V_RF (V)
ΔV_out / V_logic
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

Fig. 14

Fig. 1 Four examples of ESD protection circuit topologies: (a) ground to signal ESD diode, (b) diffused resistance and signal to Vdd ESD diode, (c) gate grounded NMOS and PMOS, and (d) zener topology with two diodes from ground to signal separated by a diffused resistor and back to back zeners from signal to Vdd.

Fig. 2 Block diagram of (a) the input to a CMOS inverter including parasitic inductance (L_p), ESD protection diodes and an inverter stage and (b) simple model for ESD protection diode modeled as a voltage dependent junction capacitance (C_j), voltage dependent video resistance R_v, and current spreading resistance (R_s).

Fig. 3 The measured I-V characteristics of ESD diodes from ground to signal lines for the HCT and LVX inverters fit to the ideal diode equation to determine saturation current (I_s) and emission coefficient (n).

Fig. 4 Junction capacitance measured using a HP 8722D VNA and calculated for the ESD protection diode from ground to signal line in the LVX CMOS inverter fit to the voltage dependent junction capacitance to determine (C_{j0}) and the p-n grading coefficient (m).

Fig. 5 Block diagram for circuit used to measure the rectified input and resulting output voltage for the 74HCT04. A Stanford Research Systems DG535 was used as an external pulse source for the Agilent E4438C Vector Signal Generator. The RF pulses were capacitively coupled to the input of the 74HCT04 for the injection experiments. A 100 MHZ low-pass filter (LPF) was used to measure the low-frequency rectified voltage at the input of the HCT CMOS inverter via a Tektronix TDS 540C oscilloscope. The same oscilloscope also captured the time domain waveforms of the RF envelope pulse and the output voltage.

Fig. 6 PSPICE circuit diagram of the CMOS inverter used to simulate the drive curve and time domain waveforms of a HCT CMOS inverter. The ESD protection

topology consists of two diodes separated by a diffusion resistor. The low-frequency rectified voltage was monitored through the low-pass network.

Fig. 7 The measured input drive curve for the HCT CMOS inverter when a low bias voltage (0.0 volts) and high bias (3.0 volts) were applied which was fit to the simulated drive curve in the circuit of Fig. 6.

Fig. 8 PSPICE circuit diagram of the CMOS inverter used to simulate the drive curve and time domain waveforms of a LVX CMOS device. The ESD protection topology consists of a diode from signal to ground and a diode from signal to Vdd. The low-frequency rectified voltage was monitored through the low-pass network.

Fig. 9 The measured input drive curve for the LVX CMOS inverter when no bias voltage was applied which was fit to the simulated drive curve in the circuit of Fig. 8.

Fig. 10 Plots of the measured and simulated detected voltage versus load conductance for the LVX and HCT CMOS inverters.

Fig. 11 The measured rectified voltage at the input when no bias voltage was applied with the resulting output voltage (a) simulated and (b) measured on the 74HCT04 inverter. Input and output voltages are shown for RF amplitudes of 400 mV and 1 volt.

Fig. 12 The measured rectified voltage at the input when a bias voltage of three volts was applied with the resulting output voltage (a) simulated and (b) measured on the 74HCT04 inverter. Input and output voltages are shown for RF amplitudes of 400 mV and 1 volt. No state change was observed at the output in either case.

Fig. 13 Complete mapping of measured 74HCT04 inverter response versus the amplitude and frequency of pulsed RF excitation. The shading of the vertical scale indicates the fractional deviation in output voltage from the valid logic level.

Fig. 14 Map of measured 74LVX04 inverter response versus the amplitude and frequency of pulsed RF excitation.

Table I.

			Diode Models			
Parameter	**Description**	**Units**	**ESD_HCT (Lower)**	**ESD_HCT (Upper)**	**ESD_LVX (Lower)**	**ESD_LVX (Upper)**
IS	Forward Saturation Current	A	1.9E-10	1.0E-09	4.2E-12	5.0E-12
N	Emission Coefficient		1.3	1.3	1.05	1.05
RS	Current Spreading Resistance	Ω	15	20	8	20
CJO	Zero Bias Junction Capacitance	pF	2.7	2.7	2.4	2.4
M	p-n Grading Coefficient		0.3	0.3	0.3	0.3
VJ	Junction Potential	V	0.65	0.65	0.67	0.7
ISR	Recombination Current Parameter	A	1.0E-10	1.0E-10	1.0E-10	1.0E-10
TT	Transit Time (Typical Reverse Recovery Time)	s	1.0E-09	1.0E-09	1.0E-09	1.0E-09